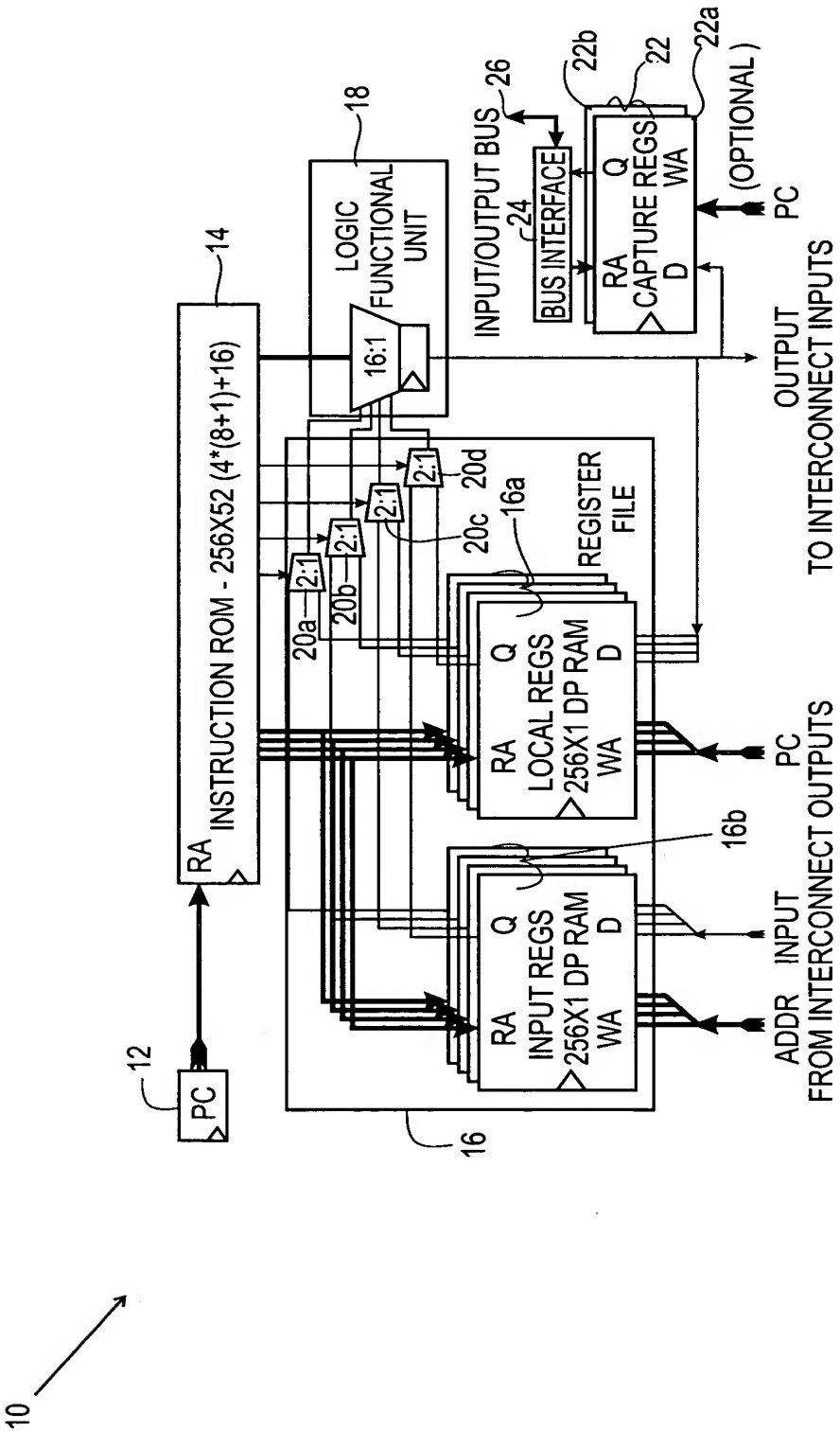


Logic Processor for programming into FPGAs
(All memories and registers are synchronously clocked by the common system clock.)

FIG. 1

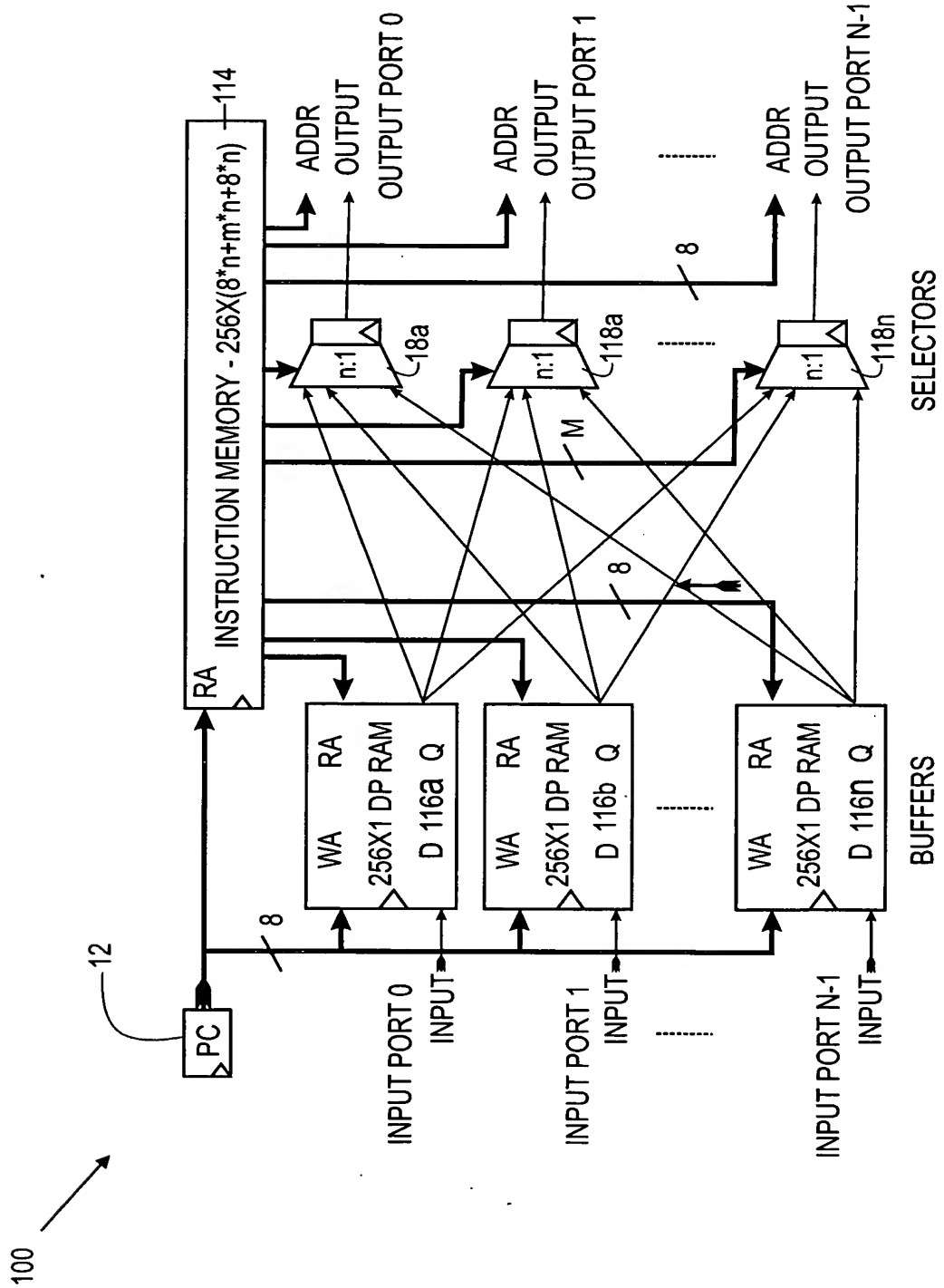
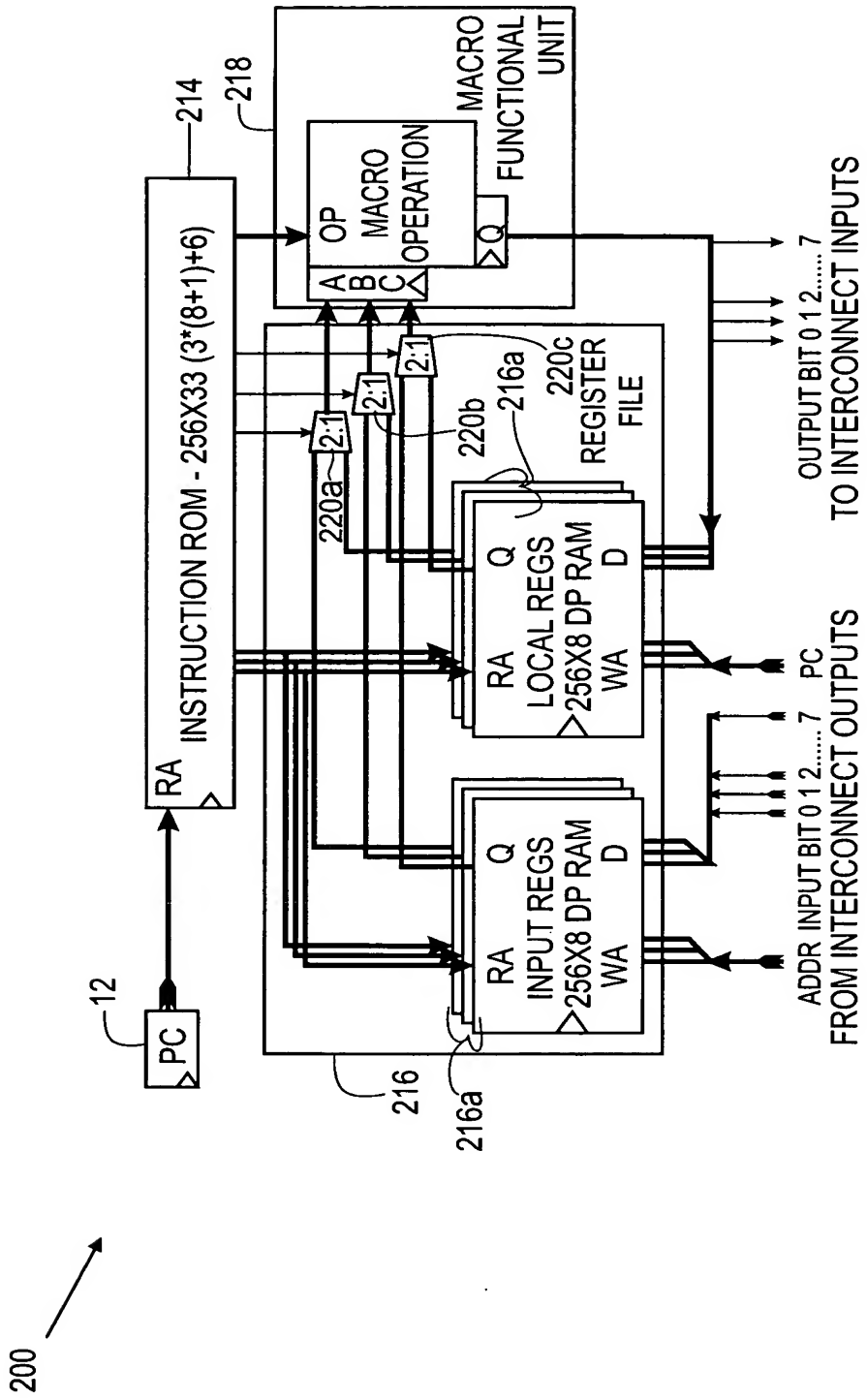

100
12
PC
8
INPUT PORT 0
INPUT
INPUT PORT 1
INPUT
INPUT PORT N-1
INPUT
WA RA
256X1 DP RAM
D 116a Q
WA RA
256X1 DP RAM
D 116b Q
WA RA
256X1 DP RAM
D 116n Q
BUFFERS
RA
INSTRUCTION MEMORY - 256X(8*n+m*n+8*n)
114
8
M
n:1
18a
118a
118n
SELECTORS
ADDR
OUTPUT
OUTPUT PORT 0
ADDR
OUTPUT
OUTPUT PORT 1
ADDR
OUTPUT
OUTPUT PORT N-1

FIG. 2



MACRO PROCESSOR

FIG. 3

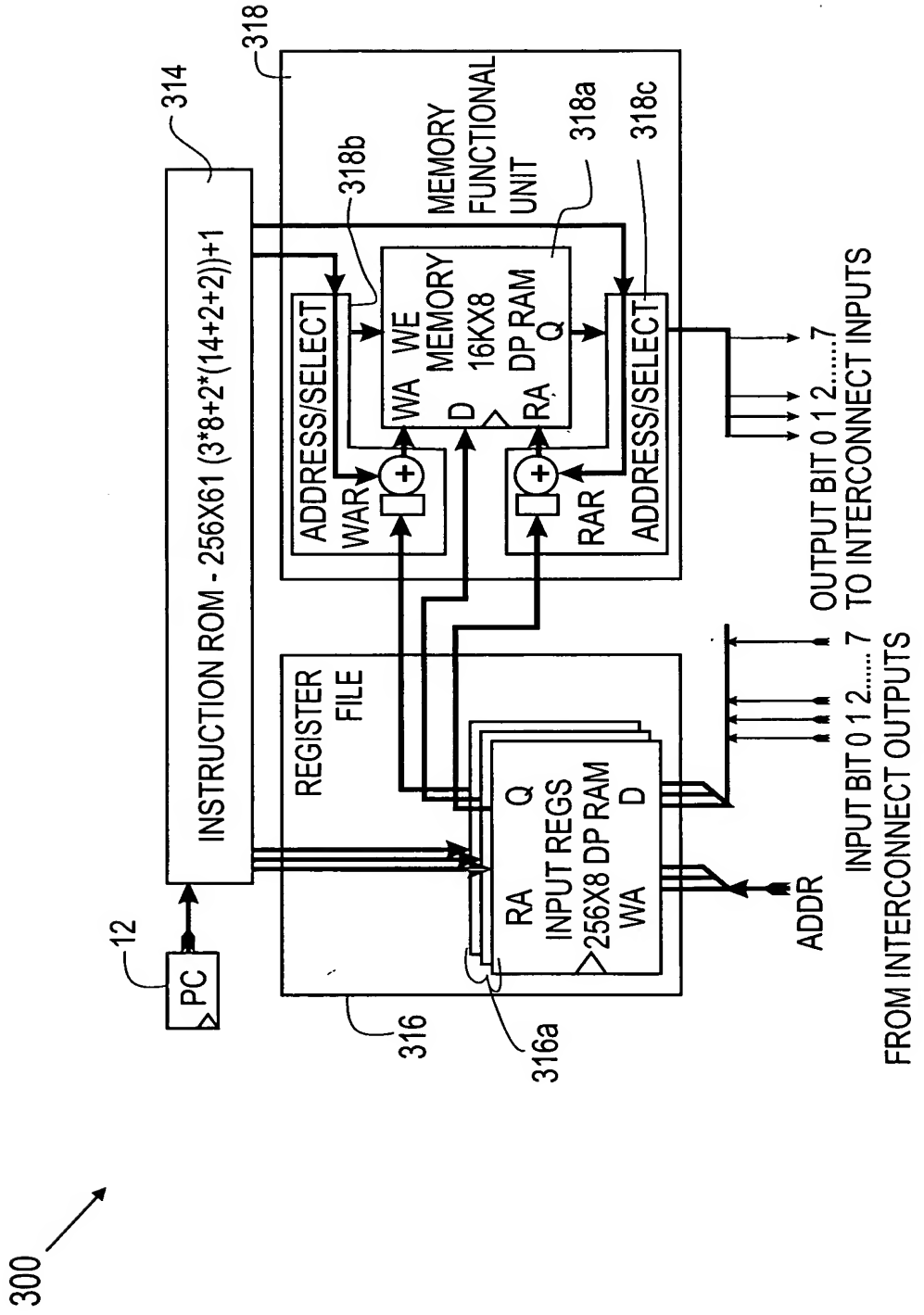

300
12
PC
314
INSTRUCTION ROM - 256X61 (3*8+2*(14+2+2))+1
316
REGISTER FILE
316a
RA
INPUT REGS
256X8 DP RAM
WA
Q
D
ADDR
INPUT BIT 0 1 2..... 7
FROM INTERCONNECT OUTPUTS
318
MEMORY FUNCTIONAL UNIT
318a
318b
318c
ADDRESS/SELECT
WAR
WA
WE
MEMORY
16KX8
DP RAM
D
Q
RA
RAR
ADDRESS/SELECT
OUTPUT BIT 0 1 2.....7
TO INTERCONNECT INPUTS
MEMORY PROCESSOR

FIG. 4

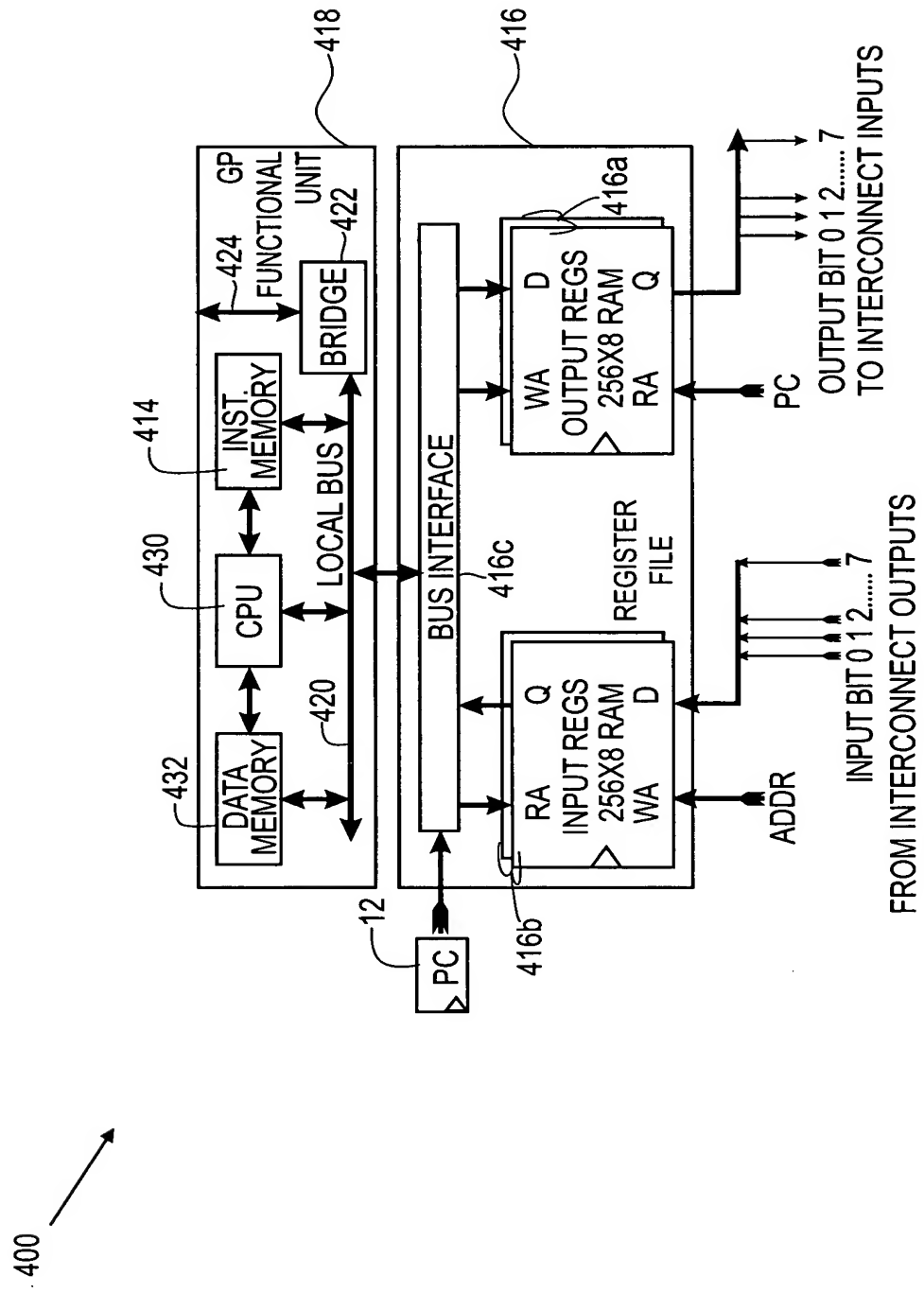

400
418
416
GP FUNCTIONAL UNIT
424
422
BRIDGE
414
INST. MEMORY
LOCAL BUS
430
CPU
420
432
DATA MEMORY
BUS INTERFACE
416c
416a
WA
OUTPUT REGS
256X8 RAM
RA
D
Q
REGISTER FILE
RA
INPUT REGS
256X8 RAM
WA
Q
D
12
PC
416b
PC
ADDR
OUTPUT BIT 0 1 2..... 7
TO INTERCONNECT INPUTS
INPUT BIT 0 1 2..... 7
FROM INTERCONNECT OUTPUTS
GENERAL PURPOSE PROCESSOR

FIG. 5

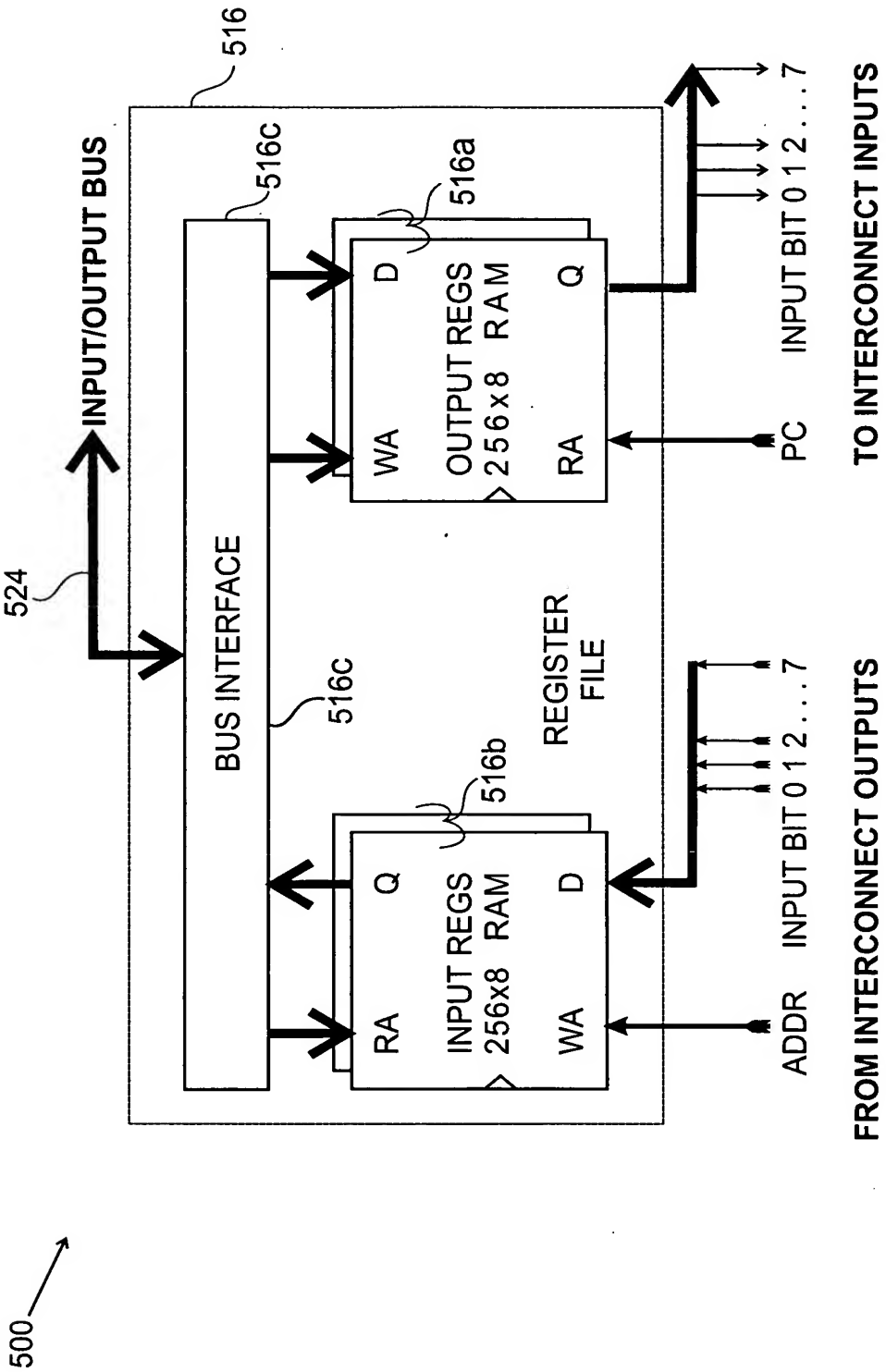

500
516
524
INPUT/OUTPUT BUS
BUS INTERFACE
516c
516c
516a
516b
REGISTER FILE
OUTPUT REGS 256x8 RAM
INPUT REGS 256x8 RAM
D
Q
WA
RA
Q
D
RA
WA
PC
ADDR
INPUT BIT 0 1 2 . . . 7
INPUT BIT 0 1 2 . . . 7
TO INTERCONNECT INPUTS
FROM INTERCONNECT OUTPUTS
INTERFACE UNIT

FIG. 6

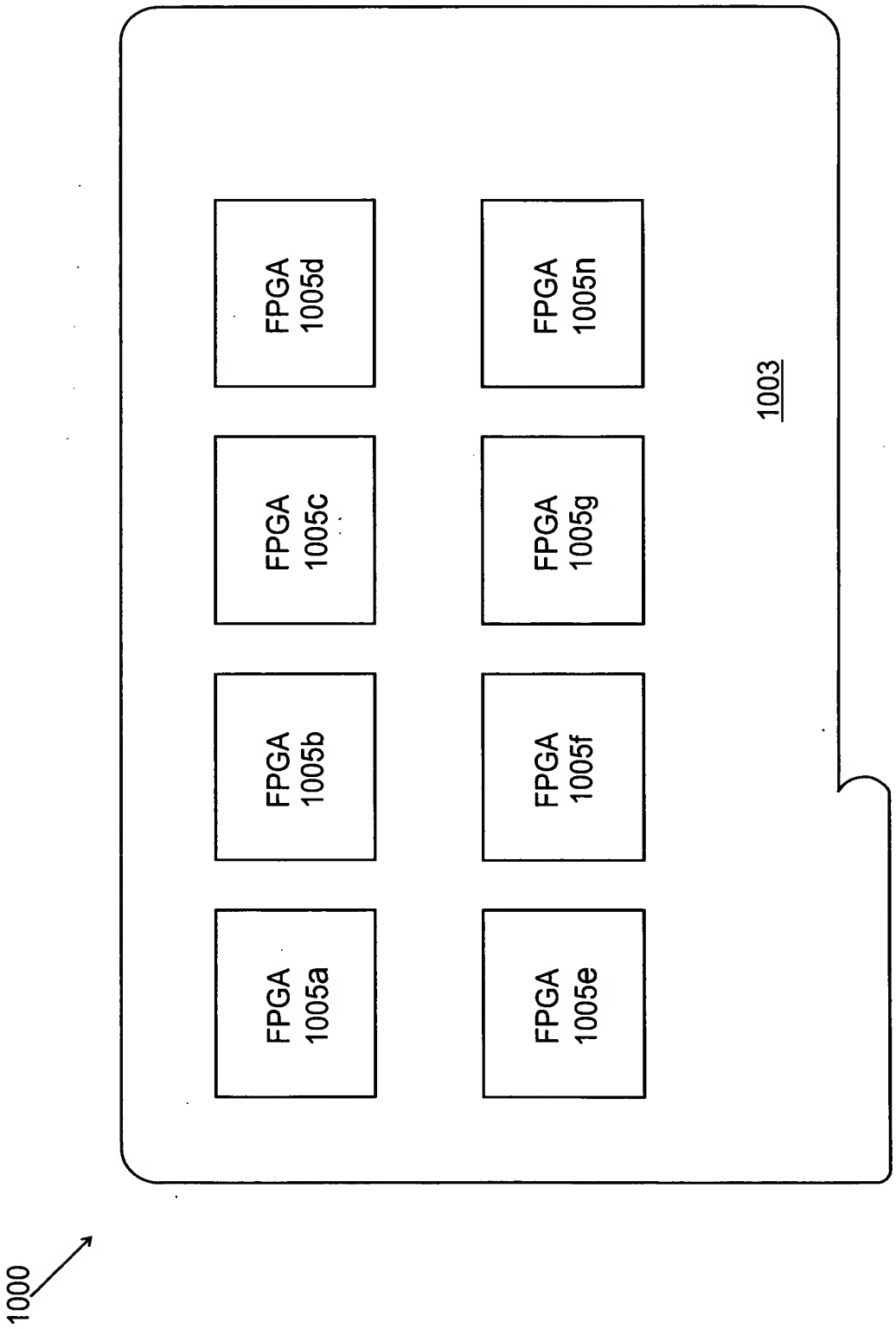

1000
1003
FPGA 1005a
FPGA 1005b
FPGA 1005c
FPGA 1005d
FPGA 1005e
FPGA 1005f
FPGA 1005g
FPGA 1005n

FIG. 7